

# Parallel Array InAs Nanowire Transistors for Mechanically Bendable, Ultrahigh Frequency Electronics

Toshitake Takahashi,<sup>†,\*,§,⊥</sup> Kuniharu Takei,<sup>†,\*,§,⊥</sup> Ehsan Adabi,<sup>†</sup> Zhiyong Fan,<sup>†,\*,§</sup> Ali M. Niknejad,<sup>†</sup> and Ali Javey<sup>†,\*,§,\*</sup>

<sup>†</sup>Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, California 94720, <sup>‡</sup>Materials Sciences Division, Lawrence Berkeley National Laboratory, Berkeley, California 94720, and <sup>§</sup>Berkeley Sensor and Actuator Center, University of California, Berkeley, California 94720. <sup>⊥</sup>These authors contributed equally to this work.

Over the past several years, semiconductor nanowires (NWs) have been extensively explored for electronic and sensor applications<sup>1–8</sup> owing to their unique physical properties with tunable and well-defined atomic composition.<sup>9</sup> In one specific platform, a contact printing technique is utilized for the large-scale assembly of NW parallel arrays on a support substrate, followed by the subsequent device fabrication.<sup>10–13</sup> Since NW arrays are utilized, the stochastic device-to-device variation is drastically reduced, which is of practical importance.<sup>14–16</sup> The performance limits of the enabled devices, however, are still unknown. In this regard, here we characterize the radio frequency (RF) response of InAs NW array transistors on bendable substrates, elucidating an important performance metric for determining their potential application domain. Notably, for the first time, the GHz operation of mechanically flexible, NW parallel array devices is demonstrated. The results demonstrate the potential of NW array devices for ultrahigh frequency (UHF) electronic circuits.

UHF electronics operating in the 0.3–3 GHz regime are highly attractive for various analog and digital circuits.<sup>17,18</sup> The ability to fabricate these devices on mechanically bendable substrates that conform nonplanar surfaces and potentially by printing techniques may further broaden their utility and application domain. In this work, highly aligned InAs NW arrays were utilized as the active channel material of the flexible, UHF field-effect transistors (FETs). InAs NWs are attractive for such applications due to their high electron mobility,<sup>2,4,19</sup> high electron saturation velocity, ease of ohmic

**ABSTRACT** The radio frequency response of InAs nanowire array transistors on mechanically flexible substrates is characterized. For the first time, GHz device operation of nanowire arrays is demonstrated, despite the relatively long channel lengths of  $\sim 1.5 \mu\text{m}$  used in this work. Specifically, the transistors exhibit an impressive maximum frequency of oscillation,  $f_{\text{max}} \sim 1.8 \text{ GHz}$ , and a cutoff frequency,  $f_t \sim 1 \text{ GHz}$ . The high-frequency response of the devices is due to the high saturation velocity of electrons in high-mobility InAs nanowires. The work presents a new platform for flexible, ultrahigh frequency devices with potential applications in high-performance digital and analog circuitry.

**KEYWORDS:** nanowires · flexible electronics · printed · plastic · radio frequency devices

metal contact formation,<sup>4,20</sup> and miniaturized diameters that make them mechanically flexible.

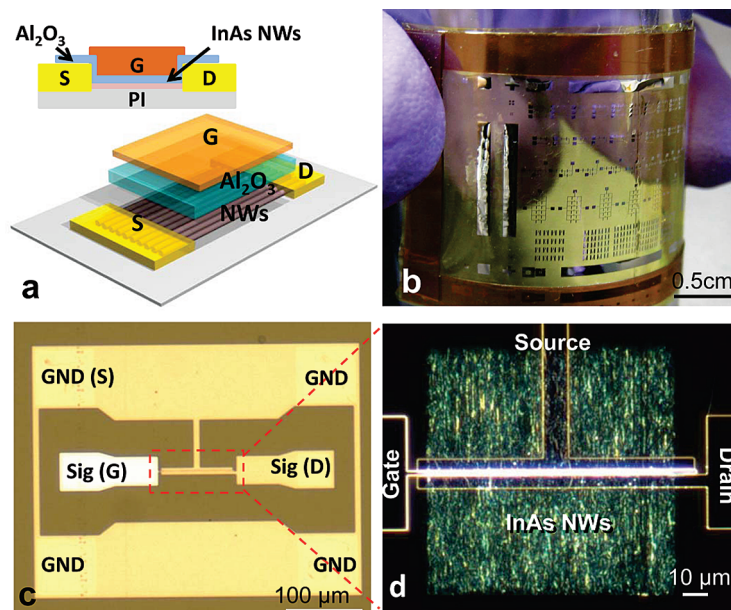
InAs NWs used in this study were synthesized on Si/SiO<sub>2</sub> substrates by a physical vapor transport method.<sup>4</sup> The grown NWs had an average diameter and length of  $\sim 30 \text{ nm}$  and  $\sim 10 \mu\text{m}$ . Subsequently, NW contact printing<sup>10,11,15</sup> was carried out by directionally sliding a growth substrate, consisting of randomly grown InAs NWs, on top of a polyimide (PI) layer (24  $\mu\text{m}$ ) spin-coated on a Si/SiO<sub>2</sub> handling wafer. During this process, NWs are directly transferred from the growth substrate to the PI surface as parallel arrays.<sup>10,11,15</sup> To achieve patterned assembly of NWs, the PI surface is first coated with a lithographically patterned resist layer, followed by NW printing and lift-off in a solvent. Nickel ( $\sim 50 \text{ nm}$ ) source (S) and drain (D) electrodes were then formed, followed by atomic layer deposition of Al<sub>2</sub>O<sub>3</sub> ( $\sim 8 \text{ nm}$ ) at 150 °C as the gate dielectric. Finally, Al (40 nm) top-gate (G) electrodes were fabricated. All electrodes were defined by photolithography and lift-off processes. There is  $\sim 200 \text{ nm}$  of misalignment due to the limitation of contact aligner,

\*Address correspondence to ajavey@berkeley.edu.

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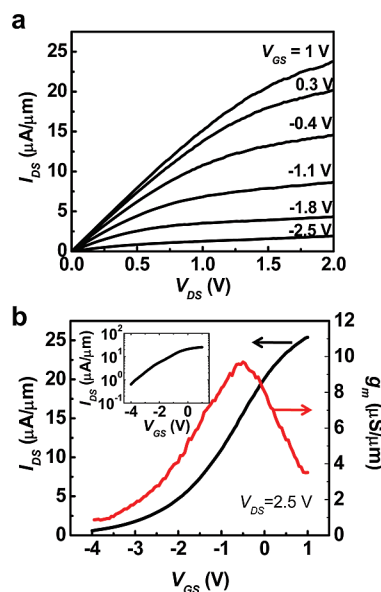


**Figure 1.** Schematic and optical images of a printed InAs NW array FET fabricated on a flexible PI substrate for GHz operation. (a) Schematic illustration of the NW parallel array FET, illustrating the various layers of the device. The cross-sectional image is shown in the top. (b) Photograph image of the fabricated NW device array on a bendable PI substrate. (c) Bright-field optical image of a NW array FET with ground–signal–ground configuration for the RF measurements. (d) Dark-field optical image, showing the printed InAs NW region.

resulting in the overlap of G with one of the S/D electrodes and underlap with the other, resulting in a parasitic capacitance and series resistance, respectively. The channel length (S/D electrode spacing) is  $L \sim 1.5 \mu\text{m}$ , and the channel width is  $W = 100\text{--}200 \mu\text{m}$ . The gate electrode length is  $L_G \sim 1.4 \mu\text{m}$ . The configuration of the electrical pads matches that of the conventional ground–signal–ground (GSG) microwave probes ( $150 \mu\text{m}$  pitch). Figure 1a shows the layered schematic of a NW array RF device. The optical microscopy images of a completed device are shown in Figure 1c,d, clearly depicting the active NW array region and the GSG electrode configuration. The printed NW density is  $\sim 4$  NWs/ $\mu\text{m}$  as confirmed by scanning electron microscopy. After the completion of the fabrication process, the PI layer is peeled off from the rigid Si/SiO<sub>2</sub> handling wafer, resulting in mechanically flexible device arrays, as shown in Figure 1b.

Figure 2a shows representative output characteristics of an InAs NW array FET with  $W = 100 \mu\text{m}$  on a flexible PI substrate. The FET delivers a unit-width normalized ON current of  $I_{\text{ON}} \sim 23 \mu\text{A}/\mu\text{m}$  at  $V_{\text{DS}} = 2 \text{ V}$ . Individual NWs with comparable lengths and diameters deliver  $\sim 10 \mu\text{A}$  of ON current based on our previous studies.<sup>4</sup> From the current density, we estimate that  $\sim 2$  NW/ $\mu\text{m}$  cross the S/D electrodes, with the rest of the NWs only contacting one electrode and thereby serving as parasitic elements (*i.e.*, they contribute to the gate capacitance but not the transconductance). A respectable ON/OFF current ratio,  $I_{\text{ON}}/I_{\text{OFF}} \sim 100$  is observed at  $V_{\text{DS}} = 2.5 \text{ V}$ , as shown in the inset of Figure 2b. From the  $I_{\text{DS}}\text{--}V_{\text{GS}}$  curve at  $V_{\text{DS}} = 2.5 \text{ V}$ , the peak transconductance,  $g_m = (dI_{\text{DS}}/dV_{\text{GS}})|_{V_{\text{DS}}} \sim 1.1 \text{ mS}$  (*i.e.*,

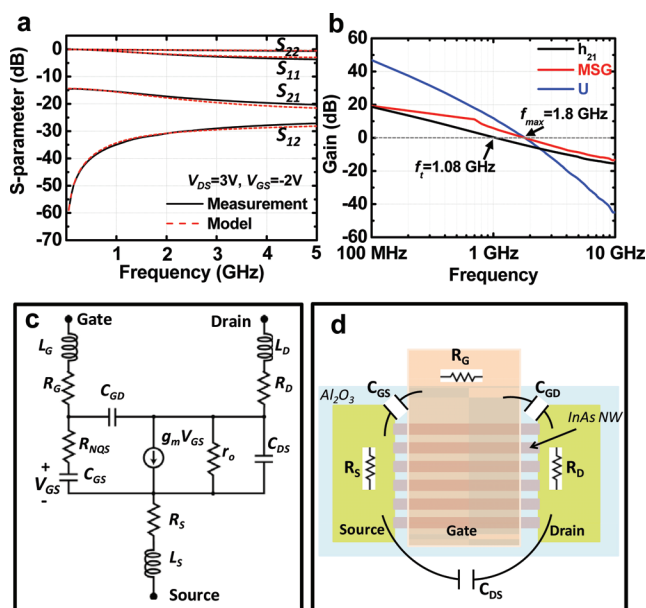
$\sim 11 \mu\text{S}/\mu\text{m}$  as normalized by  $W$ ) is measured at  $V_{\text{GS}} = -0.5 \text{ V}$  (Figure 2b). From the slope of  $I_{\text{DS}}\text{--}V_{\text{DS}}$  curve at  $V_{\text{DS}} = 2.5 \text{ V}$  and  $V_{\text{GS}} = -0.4 \text{ V}$ , the output resistance,  $r_o \sim 8 \text{ k}\Omega$  is obtained, which corresponds to a gain of  $A_v = r_o g_m \sim 8$ .  $A_v$  is the intrinsic gain of a transistor with no loading (*i.e.*, transistor is self-loaded), which is an important figure for operation amplifiers, instrumentation amplifiers, and other circuit components where large gains are desirable. Furthermore, the mechanical flex-



**Figure 2.** DC characteristics of an InAs NW array FET. (a) Normalized output characteristics of a NW array FET with a channel width,  $W \sim 100 \mu\text{m}$ , and gate length,  $L_G \sim 1.5 \mu\text{m}$ . (b) Linear-scale transfer characteristic and the corresponding transconductance as a function of gate bias at  $V_{\text{DS}} = 2.5 \text{ V}$ . The log-scale  $I_{\text{DS}}\text{--}V_{\text{GS}}$  at  $V_{\text{DS}} = 2.5 \text{ V}$  is shown in the inset.

ibility of the devices was tested by measuring the electrical properties as a function of the radius of curvature. The NW array FETs do not exhibit a significant electrical degradation, even when bent to a radius of  $\sim 18$  mm with compressive/tensile stress (see Supporting Information, Figure S1), which is attributed to the miniaturized dimensions of NWs. Additionally, since InAs NWs have significantly higher Young's modulus than the supporting PI substrate, the strain is mostly compensated by the substrate, with the strain in the NW being only  $\epsilon_{xx} \sim 0.5\%$ , as predicted from mechanical simulations (Figure S1b).

To directly extract the high-frequency behavior, the two-port scattering parameters ( $S$  parameters) of InAs NW array FETs were measured in the common-source configuration using standard procedures with a vector network analyzer (VNA) over a frequency range from 40 MHz to 10 GHz (Anritsu 37397C). Calibration of the probe tips was performed by employing the short-open-load-thru method (see Supporting Information) on an impedance standard substrate provided by Cascade Microtech (ISS 101-190). On-wafer pad-open and pad-short structures (Figure S2) were used to de-embed the parasitic effects of the contact pads, that is, shunt capacitance/conductance and series inductance/resistance (see Supporting Information for the details). This de-embedding does not correct for the overlap capacitances between the gate and source/drain electrodes. The  $S$  parameters were then used to analyze the RF performance of the device (Figure 3a).  $S_{11}$ ,  $S_{22}$ ,  $S_{21}$ , and  $S_{12}$  are, respectively, the reflection coefficient of the input, the reflection coefficient of the output, the forward transmission gain, and the reverse transmission gain. Figure 3b shows various RF metrics of a representative device with  $W = 200$   $\mu\text{m}$ , all derived from  $S$  parameters. Specifically, unity transit frequency of the current gain ( $h_{21}$ ) of a transistor is called  $f_t$  and is an important factor for determining the high-frequency limit of the transistor for various analog/RF and digital applications. To obtain  $f_t$  from the measurements,  $S$  parameters are first converted to hybrid parameters ( $h$  parameters) as described in the Supporting Information. The parameter  $h_{21}$  is plotted as a function of frequency (Figure 3b), and  $f_t$  occurs at the frequency where  $h_{21}$  equals 1, that is, 0 dB. As depicted in Figure 3b, InAs NW array FETs exhibit an impressive  $f_t = 1.08$  GHz. Maximum stable gain (MSG), the gain a transistor can provide if suitable input and output matching networks are incorporated for an unconditionally stable amplifier design, is also extracted (see Supporting Information) and plotted as a function of frequency (Figure 3b). At 1 GHz, the MSG of the FET is  $\sim 6$  dB, which confirms that designing an RF amplifier at the GHz regime is plausible. Finally, maximum unilateral gain ( $U$ , Mason gain) is extracted (Supporting Information) as a function of frequency (Figure 3b). Mason gain is the maximum unilateral power gain the device can provide at a specific frequency of opera-



**Figure 3.** RF characterization of an InAs NW array FET. (a) Measured (black solid line) and modeled (red dashed line) scattering parameters,  $S_{11}$ ,  $S_{12}$ ,  $S_{21}$ , and  $S_{22}$  of an InAs NW array FET with  $W \sim 200$   $\mu\text{m}$  after de-embedding for frequencies between 40 MHz and 5 GHz. (b) Current gain ( $h_{21}$ ), maximum stable gain (MSG), and unilateral power gain ( $U$ ) extracted from measured  $S$  parameters as a function of frequency. The unity current gain frequency,  $f_t$ , and unity power gain frequency,  $f_{max}$ , are  $\sim 1.08$  and 1.8 GHz, respectively. (c) Small signal equivalent circuit model and (d) device schematic, illustrating the various circuit components.  $R_S$ ,  $R_D$ , and  $R_G$  are composed of metal sheet resistance and contact resistance.

tion. The maximum frequency of oscillation,  $f_{max}$ , is determined by extracting Mason's gain at 0 dB. It is an important figure of merit, and at frequencies beyond  $f_{max}$  a transistor cannot provide any power gain and turns into a passive component. As shown in Figure 3b, the NW array FET has  $f_{max} = 1.8$  GHz.

A small signal model can also be fitted to the  $S$  parameter data to be used in the future circuit design and optimizations and further extract key device parameters. The small signal equivalent circuit is shown in Figure 3c,d. At the core is the hybrid- $\pi$  model of the transistor including  $g_m$ ,  $r_o$ , and the capacitances ( $C_{GS}$ ,  $C_{GD}$ , and  $C_{DS}$ ). Non-quasi-static (NQS) resistance,  $R_{NQS}$ , and the series resistance ( $R_G$ ,  $R_S$ ,  $R_D$ ) and inductance ( $L_G$ ,  $L_S$ ,  $L_D$ ) associated with the gate, source, and drain interconnects are added, resulting in the match between measured data and the fitted small signal model data (Figure 3a; see Supporting Information for details). The extracted component values for the small signal model are listed in Table 1.

To further characterize the devices,  $S$  parameters were measured at different drain and gate voltages with the extracted  $f_t$  shown in Figure 4a. As expected,  $f_t$  monotonically increases with  $V_{DS}$  for the explored bias range due to an increase in  $g_m$ . The peak  $f_t$  is obtained at  $V_{GS} = -2$  V, most likely corresponding to when the Fermi level coincides with the first conduction sub-band edge of the InAs NW channel. Due to the

**TABLE 1. Extracted and Fitted Parameters from Small Signal RF Modeling for a NW Array FET with  $W = 200 \mu\text{m}$  and  $L = 1.5 \mu\text{m}$** 

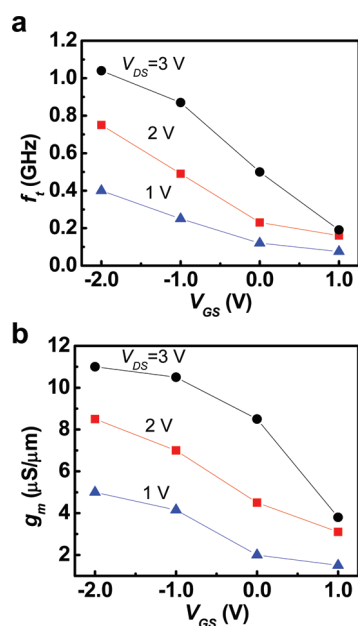
$g_m$	$r_o$	$C_{GS}$	$C_{GD}$	$C_{DS}$	$R_G$	$R_S$	$R_D$	$R_{NOS}$	$I_G$	$I_S$	$I_D$
2.3 mS	13 k $\Omega$	315 fF	35 fF	10 fF	102 $\Omega$	66 $\Omega$	73 $\Omega$	85 $\Omega$	200 pH	92 pH	148 pH

nonparabolicity of the band structure, effective mass increases as the Fermi level goes deeper into the conduction band, thereby lowering the electron mobility and saturation velocity. Since cutoff frequency is proportional to saturation velocity, it follows that as higher positive gate voltages,  $f_t$  decreases. Similarly,  $g_m$  can be extracted as a function of bias from the RF measurements (Figure 4b). A peak transconductance of  $g_m \sim 12 \mu\text{S}/\mu\text{m}$  at  $V_{DS} = 3 \text{ V}$  and  $V_{GS} = -2 \text{ V}$  is obtained from the AC small signal RF characteristics, which is consistent with the value obtained from the DC measurements (Figure 2b). Note that the devices in Figures 2 and 4 are not the same. Due to the device-to-device variations, the threshold voltage is slightly different.

Next, we examine the theoretical performance limit of InAs NW array FETs. The cutoff frequency is projected from the relation,  $f_t = g_m/(2\pi(C_{GS} + C_{GD}))$ . In the high field operation regime (e.g., high  $V_{DS}$  and/or short  $L_G$ , as is the case in this work), the carriers propagate at the saturation velocity,  $v_{sat}$ , with the transconductance given as  $g_m = v_{sat}(C_{ox}/L_G)$ . Here  $C_{ox}$  is the gate oxide capacitance and can be obtained from  $C_{ox} = C_{ox,1} \times (Wd)$ , where  $C_{ox,1}$  is the NW gate capacitance for a single NW and  $d$  is the NW density. The cutoff frequency is then  $f_t = v_{sat}C_{ox}/(2\pi L_G(C_{GS} + C_{GD}))$ . Note that the total gate source capacitance is given as  $C_{GS} = C_{p,GS} + 2/3C_{ox}$ , where  $C_{p,GS}$  is the parasitic capacitance between G/S electrodes. The exact velocity-field curve for InAs NWs

is unknown, so we use the bulk curve for the purpose of this analysis. The cutoff frequency is then calculated by using the extracted capacitances for the explored device geometry (Table 1) and  $v_{sat} \sim 1.3 \times 10^7 \text{ cm/s}$  at a field of 16 kV/cm (corresponding to  $V_{DS} = 2.5 \text{ V}$  and  $L_G = 1.5 \mu\text{m}$ ).<sup>21</sup> From this analysis,  $f_t \sim 7 \text{ GHz}$  is projected for  $d = 2 \text{ NWs}/\mu\text{m}$  (Figure S4, Supporting Information) and  $L_G = 1.5 \mu\text{m}$ , which is  $\sim 7$  times higher than the experimental  $f_t$  for the same NW density. This may be attributed to the dominant role of surface scattering in the electron transport properties of unoptimized InAs NWs used in this work. In the future, exploration of surface passivation layers may help to further enhance the measured frequency response of NW RF-FETs. Additionally, by increasing the printed NW density to 20 NWs/ $\mu\text{m}$  (50 nm pitch), the theoretical  $f_t$  increases to  $\sim 13 \text{ GHz}$ . Finally, in the absence of all parasitic elements, an ultimate theoretical  $f_t$  of  $\sim 14 \text{ GHz}$  is projected, presenting the “intrinsic” cutoff frequency of the InAs transistors at the explored length scales. Further gate length miniaturization can also enhance the RF performance.

The GHz operation of our FETs compares favorably with the other previously explored flexible device concepts. For example, hydrogen-terminated amorphous silicon or silicon films with various degrees of crystallinity have been widely utilized for applications in large-scale electronics with the highest reported  $f_t$  of  $\sim 250 \text{ MHz}$  on plastic substrates.<sup>22</sup> Organic transistors have been limited to  $f_t$  of  $\sim 10 \text{ MHz}$ <sup>23</sup> due to their low carrier mobilities. Several groups have achieved GHz operation using carbon nanotube arrays on either a plastic or rigid substrate<sup>17,24–27</sup> and graphene on a rigid substrate.<sup>28</sup> However, these devices exhibit poor  $I_{ON}/I_{OFF}$  due to the mixture of metallic nanotubes in the arrays and the small band gap of graphene. Previous work utilizing NWs for flexible electronics resulted in devices operating at 10–100 MHz,<sup>29–31</sup> although higher frequencies have been reported for single NWs with short channels on rigid Si substrates.<sup>32</sup> Egard *et al.*<sup>33</sup> recently reported GHz devices with  $f_t > 7 \text{ GHz}$  and  $f_{max} > 20 \text{ GHz}$  based on vertical InAs NW arrays grown epitaxially on InP wafers with a gate length of  $\sim 100 \text{ nm}$ . This work shows the potential of InAs NWs for high-frequency transistors; however, the explored structure and geometry are not compatible with flexible electronics. Recently, promising flexible devices<sup>34</sup> are reported using inorganic single-crystalline flakes such as Si ( $f_t \sim 0.5–3 \text{ GHz}$  for  $L_G \sim 2 \mu\text{m}$ )<sup>35,36</sup> and GaAs ( $f_t \sim 1.5 \text{ GHz}$  for  $L_G \sim 2 \mu\text{m}$ ).<sup>37</sup> These devices are fabricated *via* top-down etching and subsequent transfer method. The RF NW



**Figure 4.** Bias dependence of the RF response. (a,b) Measured unity current gain frequency and transconductance as a function of  $V_{GS}$  and  $V_{DS}$  for a NW array FET with  $W = 200 \mu\text{m}$ .



device concept presented here has the advantage of potentially utilizing an all-printed fabrication scheme, without the need for complex lithographic processes.

The presented results show the potential of NW array FETs for future microwave applications on nonconventional substrates as enabled by (i) the uniform and dense assembly of NW parallel arrays, (ii) the inherently high saturation velocity of InAs, and (iii) the appropriate device design. This technology is of particular interest given the recent rapid growth of signal communication over the UHF bands. Notably, the explored device dimensions are within the resolution limit of advanced printing processes,<sup>38</sup> thereby making the presented platform potentially compatible with continuous roll-to-roll fabrication processes. In the future, further miniaturization of the device dimensions, improved printed NW array densities, and the use of surface passivation layers through process optimization are projected to enhance the cutoff frequency of the devices by an additional ~10-fold. This projected performance cap is comparable to that of the state-of-the-art nanoscale Si devices but uniquely is attainable on nonrigid substrates and with all-printed fabrication processes.

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**Supporting Information Available:** Mechanical bendability of NW array FETs; details of de-embedding pad parasitic; extraction of  $h_{21}$ , MSG, and  $U$  from the  $S$  parameters; hybrid- $\pi$  model; the effect of NW density on extrinsic cutoff frequency. This material is available free of charge via the Internet at <http://pubs.acs.org>.

## REFERENCES AND NOTES

- Xiang, J.; Lu, W.; Hu, Y.; Wu, Y.; Yan, H.; Lieber, C. M. Ge/Si Nanowire Heterostructures as High-Performance Field-Effect Transistors. *Nature* **2006**, *441*, 489–493.
- Bryllert, T.; Wernersson, L. E.; Froberg, L. E.; Samuelson, L. Vertical High-Mobility Wrap-Gated InAs Nanowire Transistor. *IEEE Electron Device Lett.* **2006**, *27*, 323–325.
- Wang, D.; Sheriff, B.; Heath, J. R. Complementary Symmetry Silicon Nanowire Logic: Power-Efficient Inverters with Gain. *Small* **2006**, *2*, 1153–1158.
- Ford, A. C.; Ho, J. C.; Chueh, Y.-L.; Tseng, Y.-C.; Fan, Z.; Guo, J.; Bokor, J.; Javey, A. Diameter-Dependent Electron Mobility of InAs Nanowires. *Nano Lett.* **2009**, *9*, 360–365.
- Ju, S.; Facchetti, A.; Xuan, Y.; Liu, J.; Ishikawa, F.; Ye, P.; Zhou, C.; Marks, T. J.; Jane, D. B. Fabrication of Fully Transparent Nanowire Transistors for Transparent and Flexible Electronics. *Nat. Nanotechnol.* **2007**, *2*, 378–384.
- Ju, S.; *et al.* Transparent Active Matrix Organic Light-Emitting Diode Displays Driven by Nanowire Transistor Circuitry. *Nano Lett.* **2008**, *8*, 997–1004.
- Stern, E.; Klemic, J. F.; Routenberg, D. A.; Wyrembak, P. N.; Turner-Evans, D. B.; Hamilton, A. D.; LaVan, D. A.; Fahmy, T. M.; Reed, M. A. Label-Free Immunodetection with CMOS-Compatible Semiconducting Nanowires. *Nature* **2007**, *445*, 519–522.
- Cohen-Karni, T.; Timko, B. P.; Weiss, L. E.; Lieber, C. M. Flexible Electrical Recording from Cells Using Nanowire Transistor Arrays. *Proc. Natl. Acad. Sci. U.S.A.* **2009**, *106*, 7309–7313.
- Lieber, C. M.; Wang, Z. L. Functional Nanowires. *MRS Bull.* **2007**, *32*, 99.
- Yerushalmi, R.; Jacobson, Z. A.; Ho, J. C.; Fan, Z.; Javey, A. Large Scale, Highly Ordered Assembly of Nanowire Parallel Arrays by Differential Roll Printing. *Appl. Phys. Lett.* **2007**, *91*, 203104.
- Fan, Z.; Ho, J. C.; Jacobson, Z. A.; Yerushalmi, R.; Alley, R. L.; Razavi, H.; Javey, A. Wafer-Scale Assembly of Highly Ordered Semiconductor Nanowire Arrays by Contact Printing. *Nano Lett.* **2008**, *8*, 20–25.
- Takahashi, T.; Takei, K.; Ho, J. C.; Chueh, Y.-L.; Fan, Z.; Javey, A. Monolayer Resist for Patterned Contact Printing of Aligned Nanowire Arrays. *J. Am. Chem. Soc.* **2009**, *131*, 2102–2103.
- Fan, Z.; Ho, J. C.; Takahashi, T.; Yerushalmi, R.; Takei, K.; Ford, A. C.; Chueh, Y.-L.; Javey, A. Towards the Development of Printable Nanowire Electronics and Sensors. *Adv. Mater.* **2009**, *21*, 3730–3743.
- Javey, A.; Nam, S.; Friedman, R. S.; Yan, H.; Lieber, C. M. Layer-by-Layer Assembly of Nanowires for Three-Dimensional, Multifunctional Electronics. *Nano Lett.* **2007**, *7*, 773–777.
- Fan, Z.; Ho, J. C.; Jacobson, Z. A.; Razavi, H.; Javey, A. Large Scale, Heterogeneous Integration of Nanowire Arrays for Image Sensor Circuitry. *Proc. Natl. Acad. Sci. U.S.A.* **2008**, *105*, 11066–11070.
- Takei, K.; Takahashi, T.; Ho, J. C.; Ko, H.; Gillies, A. G.; Leu, P. W.; Fearing, R. S.; Javey, A. Nanowire Active Matrix Circuitry for Low-Voltage Macro-Scale Artificial Skin. *Nat. Mater.* DOI: 10.1038/NMAT2835.
- Rutherglen, C.; Jain, D.; Burke, P. J. Nanotube Electronics for Radiofrequency Applications. *Nat. Nanotechnol.* **2009**, *4*, 811–819.
- Schwierz, F.; Liou, J. J. RF Transistors: Recent Developments and Roadmap toward Terahertz Applications. *Solid-State Electron.* **2007**, *51*, 1079–1091.
- Dayeh, S. A.; Aplin, D. P. R.; Zhou, X.; Yu, P. K. L.; Yu, E. T.; Wang, D. High Electron Mobility InAs Nanowire Field-Effect Transistors. *Small* **2007**, *3*, 326–332.
- Chueh, Y.-L.; Ford, A. C.; Ho, J. C.; Jacobson, Z. A.; Fan, Z.; Chen, C.-Y.; Chou, L.-Y.; Javey, A. Formation and Characterization of Ni<sub>x</sub>InAs/InAs Nanowire Heterostructures by Solid Source Reaction. *Nano Lett.* **2008**, *8*, 4528–4533.
- Brennan, K.; Hess, K. High Field Transport in GaAs, InP and InAs. *Solid-State Electron.* **1984**, *27*, 347–357.
- Kane, M. G.; Goodman, L.; Firester, A. H.; van der Wilt, P. C.; Limanov, A. B.; Im, J. S. 100 MHz CMOS Circuits Using Sequential Laterally Solidified Silicon Thin-Film Transistors on Plastic. *Tech Dig. - Int. Electron Devices Meet.* **2005**, 939–941.
- Dodabalapur, A. Organic and Polymer Transistors for Electronics. *Mater. Today* **2006**, *9*, 24–30.
- Chimot, N.; Derycke, V.; Goffman, M. F.; Bourgoin, J. P.; Happy, H.; Dambine, G. Gigahertz Frequency Flexible Carbon Nanotube Transistors. *Appl. Phys. Lett.* **2007**, *91*, 153111.
- Kocabas, C.; *et al.* High-Frequency Performance of Submicrometer Transistors That Use Aligned Arrays of Single-Walled Carbon Nanotubes. *Nano Lett.* **2009**, *9*, 1937–1943.
- Close, G. F.; Yasuda, S.; Paul, B.; Fujita, S.; Wong, H.-S. P. A 1 GHz Integrated Circuit with Carbon Nanotube Interconnects and Silicon Transistors. *Nano Lett.* **2008**, *8*, 706–709.
- Rosenblatt, S.; Lin, H.; Sazonova, V.; Tiwari, S.; McEuen, P. L. Mixing at 50 GHz Using a Single-Walled Carbon Nanotube Transistor. *Appl. Phys. Lett.* **2005**, *87*, 153111.
- Lin, Y. M.; Dimitrakopoulos, C.; Jenkins, K. A.; Farmer, D. B.; Chiu, H.-Y.; Grill, A.; Avouris, P. 100-GHz Transistors from Wafer-Scale Epitaxial Graphene. *Science* **2010**, *327*, 622–625.

29. Friedman, R. S.; McAlpine, M. C.; Ricketts, D. S.; Ham, D.; Lieber, C. M. High-Speed Integrated Nanowire Circuits. *Nature* **2005**, *434*, 1085.
30. Nam, S. W.; Jiang, X.; Xiong, Q.; Ham, D.; Lieber, C. M. Vertically Integrated, Three-Dimensional Complementary Metal-Oxide-Semiconductor Circuits. *Proc. Natl. Acad. Sci. U.S.A.* **2009**, *106*, 21035–21038.
31. Dattoli, E. N.; Kim, K.-H.; Fung, W. Y.; Choi, S.-Y.; Lu, W. Radio Frequency Operation of Transparent Nanowire Thin-Film Transistors. *IEEE Electron Device Lett.* **2009**, *30*, 730–732.
32. Vandembrouck, S.; Madjour, K.; Theron, D.; Dong, Y. J.; Li, Y.; Lieber, C. M.; Gaquiere, C. 12 GHz F-MAX GaN/AlN/AlGaN Nanowire MISFET. *IEEE Electron Device Lett.* **2009**, *30*, 322–324.
33. Egard, M.; Johansson, S.; Johansson, A.-C.; Persson, K.-M.; Dey, A. W.; Borg, B. M.; Thelander, C.; Wernersson, L.-E.; Lind, E. Vertical InAs Nanowire Wrap Gate Transistors with  $f_t > 7$  GHz and  $f_{max} > 20$  GHz. *Nano Lett.* **2010**, *10*, 809–812.
34. Rogers, J. A.; Huang, Y. A Curvy, Stretchy Future for Electronics. *Proc. Natl. Acad. Sci. U.S.A.* **2009**, *106*, 10875–10876.
35. Ahn, J. H.; Kim, H.-S.; Lee, K. J.; Zhu, Z.; Menard, E.; Nuzzo, R. G.; Rogers, J. A. High-Speed Mechanically Flexible Single-Crystal Silicon Thin-Film Transistors of Plastic Substrates. *IEEE Electron Device Lett.* **2006**, *27*, 460–462.
36. Yuan, H.-C.; Ma, Z. Microwave Thin-Film Transistors Using Si Nanomembranes on Flexible Polymer Substrate. *Appl. Phys. Lett.* **2006**, *89*, 212105.
37. Sun, Y.; Menard, E.; Rogers, J. A.; Kim, H.-S.; Kim, S.; Chen, G.; Adesida, I.; Dettmer, R.; Cortez, R.; Tewksbury, A. Gigahertz Operation in Flexible Transistors on Plastic Substrates. *Appl. Phys. Lett.* **2006**, *88*, 183509.
38. Park, J.-U.; *et al.* High-Resolution Electrohydrodynamic Jet Printing. *Nat. Mater.* **2007**, *6*, 782–789.